These are procedures for RF Layout Design in Altium:

General Outline:

1. Define DRC Rules
2. Define layer stackup
3. Use impedance calculator to determine sizing (mainly width) of trace(s) for 50 Ohm impedance
4. Draw everything, do your PCB design, etc.
5. Define net classes to categorize traces
6. Set DRC rules for clearance and lengths that reference the net classes
    a. Use interactive trace length tuner for length matching
7. Do co-planar polygon pours (with now defined clearance rules, etc.)
8. Apply gnd via stitching with spacing that is small enough to avoid RF resonances

1. Define DRC Rules

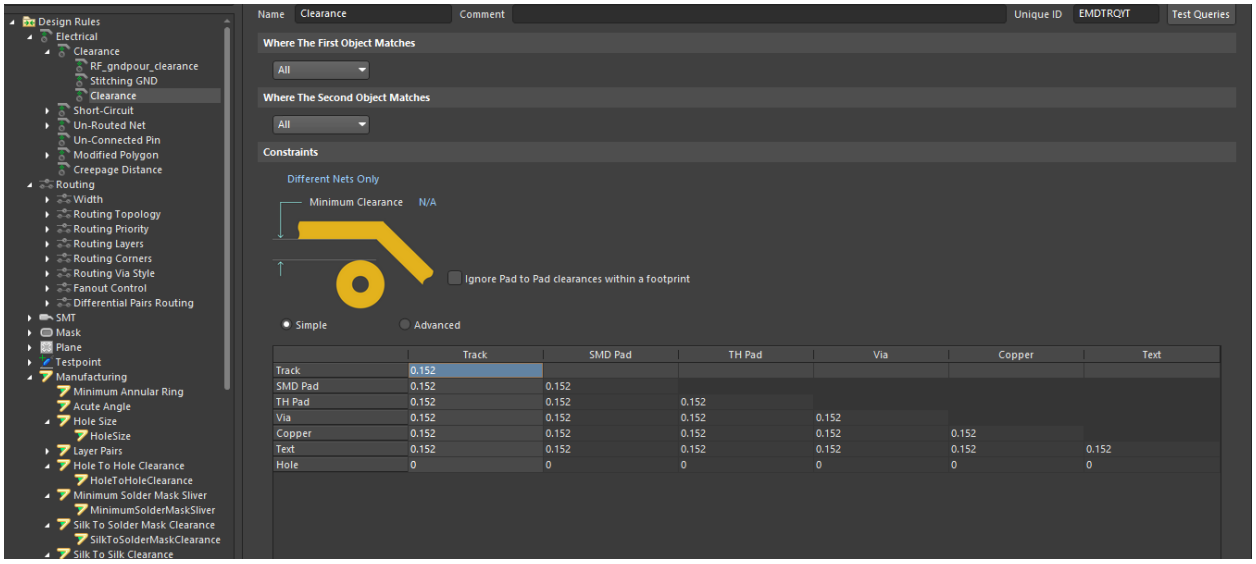
There are various DRC rules in general. However, in most cases you will only need to deal with one, which is clearance.

Go to DESIGN → RULES.. → Electrical → Clearance

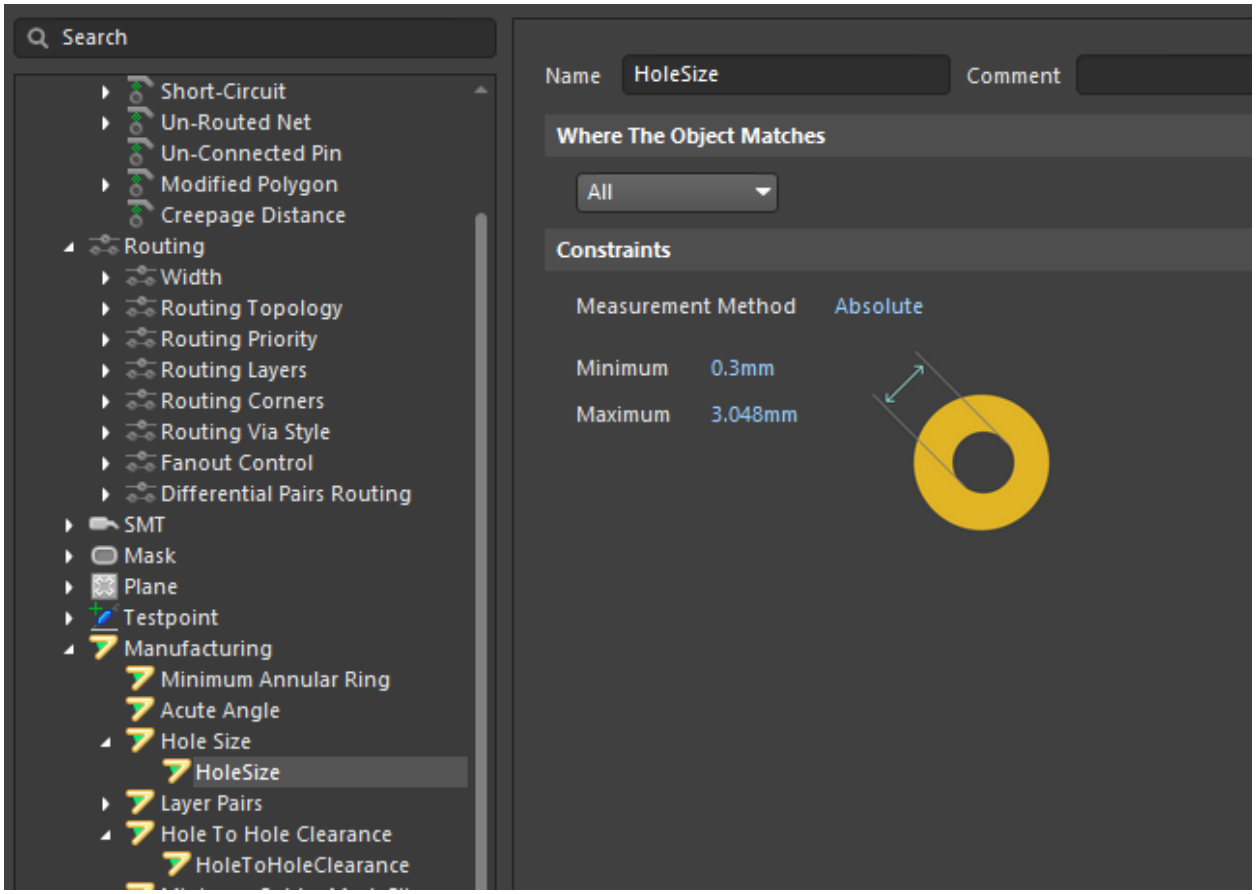
Double click into the clearance design rule and set the clearance rules from the fabricators website typically under capabilities. This may be the best case. Look at the quote section to see the different tolerance rules you can select from. **Usually the minimum clearance is overkill and more expensive.**

The two main specifications you should look out for are Min. Trace Width, Min Trace Space (sometimes clubbed together), and Min. Hole Size.

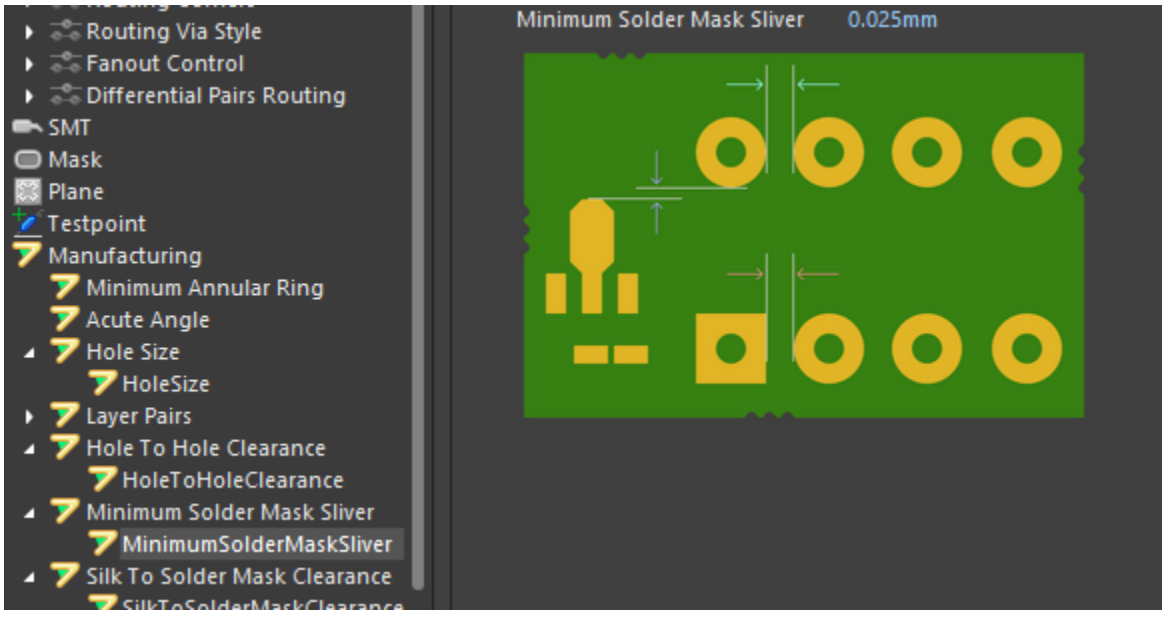
Below is an example of a Min. Trace/Space selected as 6mils (~0.152mm) in the quote section of PCBMinions (as of Aug 4, 2022). Therefore, I defined all the relevant dimensions as such in the Clearance DRC as seen below:



Furthermore, inder Manufacturing rule section, you can change the hold size design rule to the hole size requirement for your fabrication. In my example, I chose 0.3mm based on my quote selection from PCBMinions as seen below:



Another relevant DRC to keep an eye out for is soldermask sliver. This determines how little of solder mask you can have between two pads, etc. Since this was somewhat poorly explained, an image from the DRC rule is provided to better portray the rule:



This will likely be more relevant if you are dealing with very small components and may be problematic between pads of a component. Most likely, this rule may mostly be accounted for through the clearance rules which set how far separated pads can be from each other, but occasionally may not. **This rule is also not always outlined by the fabricator. Emailing the fabricator may be a good option. In all honesty, this rule may not be problematic in most cases. You may be able to get away with submitting your PCB's GDSII files with the default soldermask sliver rule.** *If there is a problem somewhere the fabricator will reach back to you and tell you the issue and where it is, which can then be fixed and resubmitted.*

2. Define Layer Stackup:

Design → Layer Stack Manager

From here the following will show up (likely 2 layers by default). Can change the names, material, copper weight based on what the fabricator specifications are. Note, in PCB design, the thickness is defined through the weight of copper. Also, in type, define whether a layer is a routing layer ('signal') or a ground plane or power plane ('Plane'). **To get exact data, you should email the fabricator for their layer stack.**

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.01016mm	3.5	
1	Top Layer		Signal	1oz	0.035mm		
	Dielectric 2	PP-022	Prepreg		0.175mm	4.2	0.02
2	TOP_GND	CF-004	Plane	1oz	0.035mm		
	Dielectric 1	FR-4	Dielectric		1.13mm	4.2	
3	BOT_GND	CF-004	Plane	1oz	0.035mm		
	Dielectric 3	PP-022	Prepreg		0.175mm	4.2	0.02
4	Bottom Layer		Signal	1oz	0.035mm		
	Bottom Solder	Solder Resist	Solder Mask		0.01016mm	3.5	
	Bottom Overlay		Overlay				

The above image is an example of specifications for a 4-layer board from PCB Minions as of Aug 4, 2022. Likely this should be the same, but may want to double check that it has not changed.

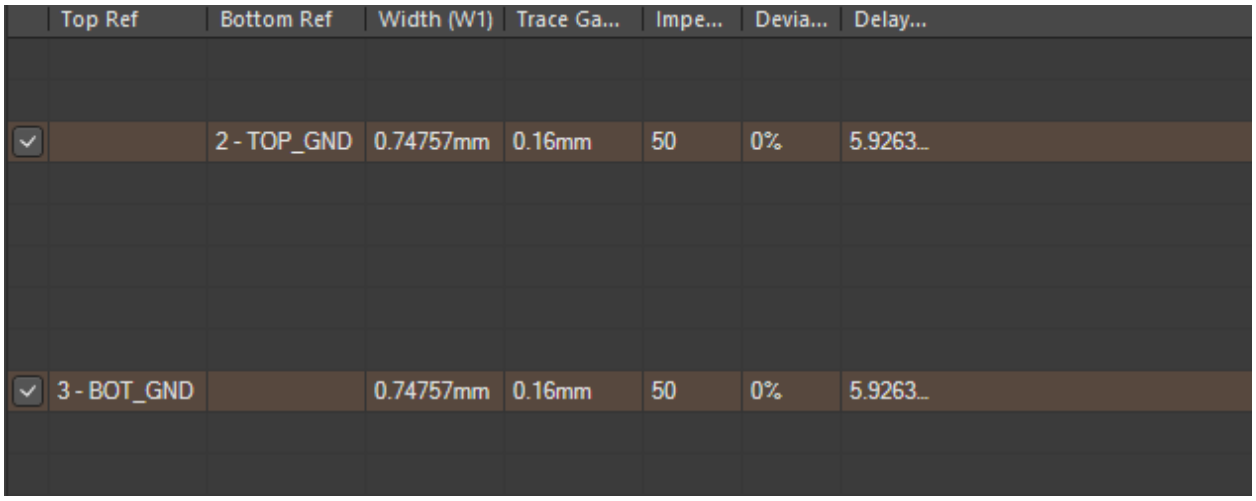
3. Impedance Calculation

From the Layer Stack Manager, see near the bottom left. There should be three tabs: stackup, impedance, via types. *Select Impedance.*

DO NOT CLOSE THE PROPERTIES POPUP WINDOW.

If displayed, click ADD IMPEDANCE PROFILE on the window to the right of the stackup. This should provide various options of combinations of "top reference" and "bottom reference" layers. If the entry is blank, it is likely an implied layer. For instance, if you are operating on a 4 layer board and the bottom reference is the second layer, this implies that the top layer must be layer 1 (since that is the only possible layer), and so Altium will likely leave the top layer entry blank.

An example is shown below (the accompanying layer stack is shown above in section 1):

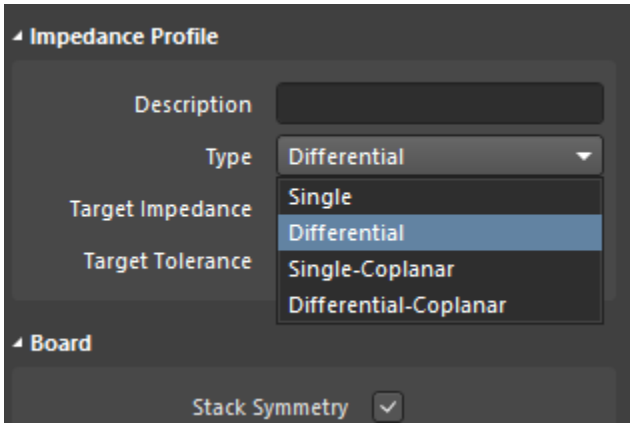


Here, you can see Top Ref is blank for the above row since that layer is implied to be 'Top Layer' from the stackup. Similarly, for the bottom row, the Bot Ref is implied to be 'Bottom Layer' from the stackup and thus is left blank.

Let's say you want to route an RF trace on the Top Layer with respect to a ground plane you have on the second layer (here called TOP_GND). Click the top row option in the impedance profiler and now the properties window/popup should reflect that you clicked that option.

IF FOR ANY REASON THE PROPERTIES WINDOW WAS CLOSED, TO THE 'PANEL' AT THE BOTTOM RIGHT AND CLICK PROPERTIES.

In the Layer Stack Manager Properties window, select the Type of routing that is being done:

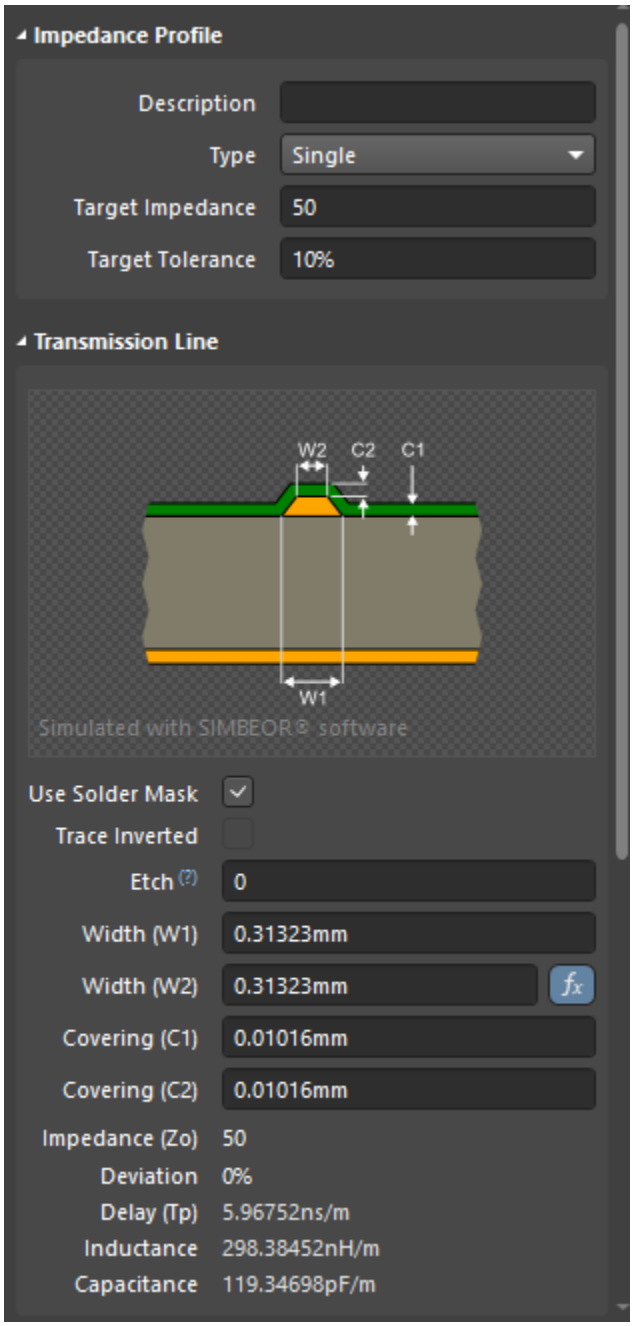


Corresponding image will be shown depicting the dimensions and trace type selected.

Most likely you will be dealing with type = single, which is basically a single microstrip over a ground plane. Type = differential may also be used, for example, after using a balun to convert RF trace from single ended to differential. In this case, the gap between the two traces will affect impedance. Nonetheless, unless doing very advanced design avoid using coplanar types.

This is because a polygon pour will be done at the end which will be the coplanar ground plane. However, I will later show a method that exploits a rule of thumb to avoid the effect of the coplanar ground plane on affecting RF trace impedance.

For now, let's consider the TYPE = SINGLE for simplicity. Simply type the target impedance (ie: 50) and the dimensions will be shown for the trace to achieve that impedance. The main dimension of interest is W1, which can be used as the width of your trace to achieve the target impedance. An example is shown below, where the required width (W1) is 0.313mm:



Note, additional information is provided which may be helpful such as Delay, inductance per unit length, and capacitance per unit length.

Keep in mind, the Layer Stackup must be defined before using this tool since it is basically a "calculator" that is taking into account the board properties.

4. PCB Layout

This section is quite vague, but I would like to mention a couple things.

Clicking TAB can be used to pause the screen and perform other tasks without moving the layout screen around. You can unpause by clicking the pause icon in the middle of the layout.

On the Layout the first thing you should do is click on the layout screen then click 'g'. This will pull up the gridding options. I like to select the smallest gridding option to allow the most free movement and placement of my cursor and objects.g

When doing your placement and routing, don't worry about the pads that are supposed to be connected to ground at this point. These ground pad connections will be automatically done at the very end when polygon pour and via stitching is completed.

When doing RF routing, I would highly recommend doing it on the top layer and having the second layer being a ground plane. This will make the RF impedance more accurately modeled and easier to design. Also, try to avoid using via's on RF routing if possible and avoid routing underneath RF traces if possible. These are all to make sure the environment the trace sees are the same and prevent possible impedance gradients/variations along the length of the trace.

At the very end of everything, even the steps after this section, apply teardrops. This can be done by TOOLS → Teardrops. I recommend making sure objects are selected as all (or selected only and have all the options selected in scope). This will help in various ways such as thermal relief, simplifying fabrication and avoiding sharp corners which may be problematic with RF paths.

In PCB design, various debates exist about acute angles and 90 deg angles in trace routing. Many of these issues may be moot in modern PCB fabrication, but nonetheless may be good design concepts. **Acute angles are to be avoided** since they can be very susceptible to the etching process (for both RF and non-RF traces). 90 deg angles at RF traces tend to cause issues since the corner can cause various problems and impedance mismatch. In our use, it may not really be a huge issue. In more legitimate RF designing, such junctions may include custom notches to account for such effects, but this is overkill for our usage. **However, such 90 deg effects are mitigated by the usage of teardrops on T-junctions, which will smoothen out the angle, making 90 deg angles good to use (for both RF and non-RF traces).**

In general it is good to keep RF paths smooth so making turns rounded or arced is a good practice. Similarly, it is best to keep an RF path straight.

Use the interactive length tuner to tune the length of traces to specific length or delay. I prefer to have the additional lengthening to be rounded rather than mitred/square etc. and have

a smaller number of cycles with a smaller radius than one big hump. *This will be more explicitly talked about later.*

For various things, it may be wise to use differential signals in the schematic level that will automate some things in the PCB level. Special things must be done and particular naming conventions are to be used for differential signals. Please look into this via Altium Forums or tutorial videos as they are not outlined in this tutorial.

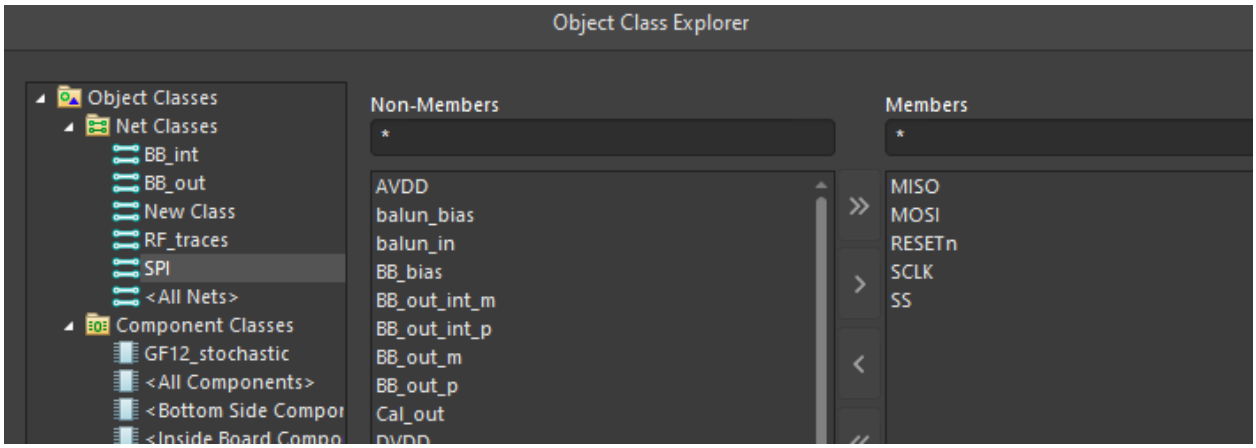
5. Define net classes to categorize traces

To prephase, I am sure there may be much better ways to do the various next steps and sections, however, this is what I have found that works and is clear (but at times could get tedious for very involved boards).

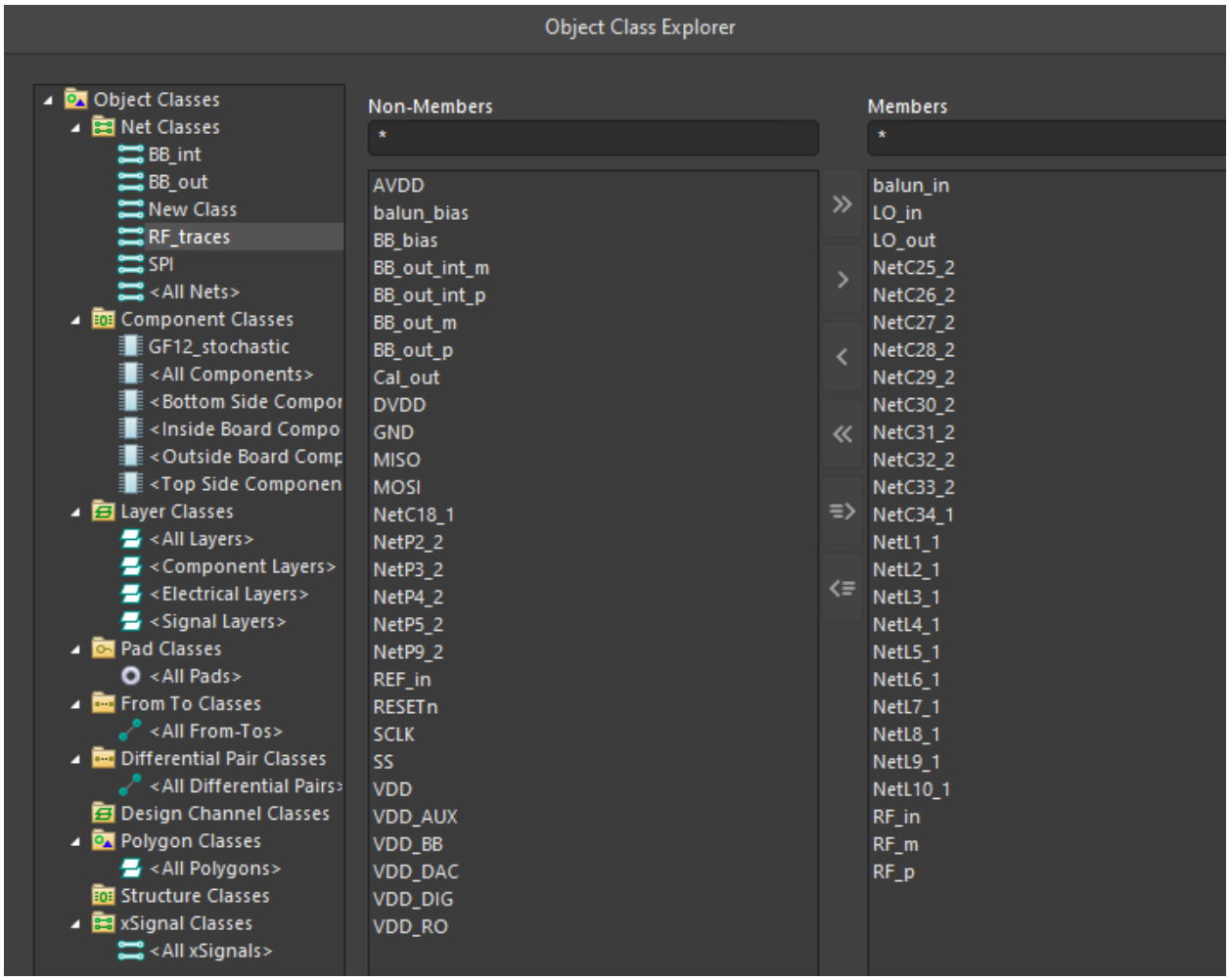
In order to assign certain properties to traces, one can use a ‘class’ to categorize a set of traces. This can later be used to define custom DRC rules for a ‘class’, which will be done in later sections.

Go to DESIGN → CLASSES…
-This will open up a window called Object Class Explorer.
-On the Net Classes dropdown, right click and ‘add class’.
-Name the class in the dropdown section
-Add the Members to the class (the members are basically the net names that you are interested in placing in a class).

An example is shown below for my SPI traces. I have MISO, MOSI, RESETn, SCLK, SS as names of net connections in my schematic and correspondingly have placed them as members in my SPI class. My goal for this particular class was to make sure trace lengths were similar to avoid possible delay mismatch that may cause SPI reading issues (although this may be overkill).



Importantly, a class should be made for any RF traces. This class will be used to define coplanar ground plane clearance from trace to avoid coupling that may change the RF trace impedance (will be discussed later). An example is shown below:



Note that I have many unnamed nets that are in the class. Your RF path may not just be one single trace (or a few traces). You must add every trace that is involved with RF signal to be in this class or else the clearance rules will not be followed for these trace locations and mess up your impedance. **All RF paths can be included in the same class**, as for what is to be done with the class is not related to what the specific RF paths are doing. *I would suggest that you manually follow the trace path and click along it to make sure you have not missed any nets.*

I tend to use classes for RF net coplanar ground clearance and differential signals for length tuning. But, classes are a nice way of defining custom DRC rules for almost anything involving a specific group of nets.

6. Make Custom DRC Rules

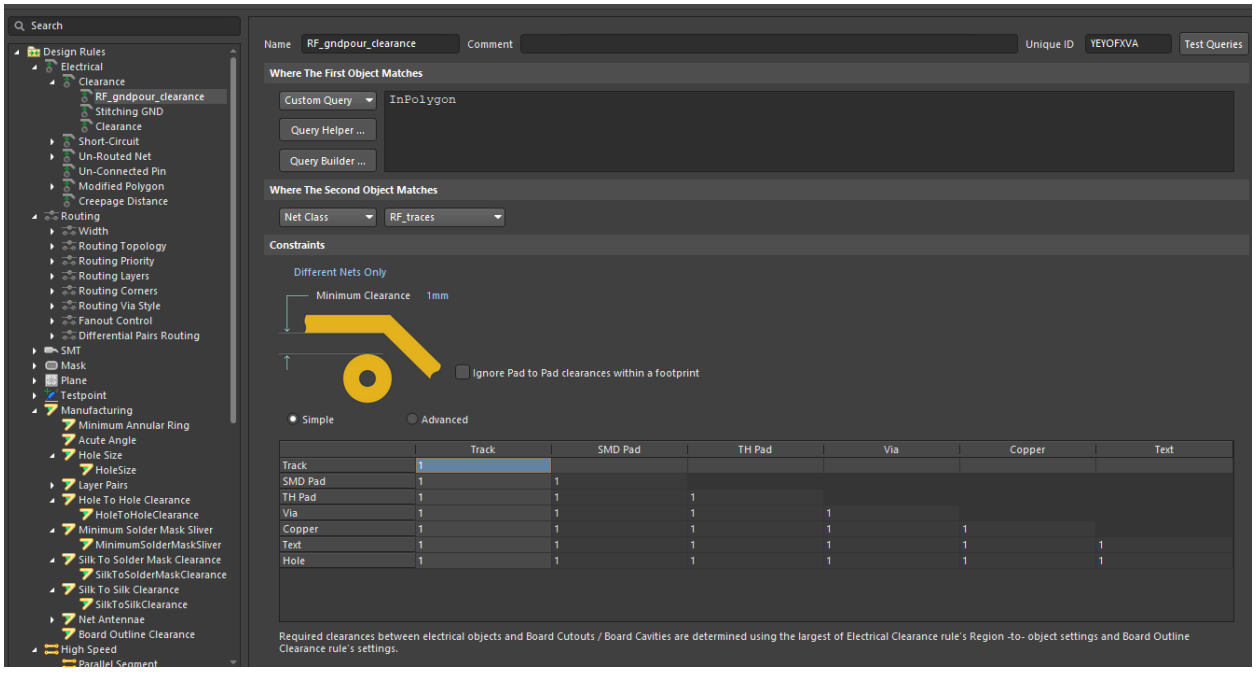
Go to DESIGN → Rules…

Then go to the Electrical → Clearance section.
Then right click the "clearance" section and create new rule
-name the rule
-click into the new rule
-Under the WHERE THE FIRST OBJECT MATCHES location, select "Custom Query" from the pulldown menu
-Enter "InPolygon" in the textbox next to the pulldown menu
-Under WHERE THE SECOND OBJECT MATCHES section select the left pulldown as "Net Class" and in the right pulldown select your RF Class (ie: RF_traces)
-Under the CONSTRAINTS section, enter the clearance

For RF traces to effectively ignore coplanar coupling that may affect the trace's impedance, keep the clearance between trace and polygon pour as 3 times the width of the RF trace.

The above 3*W rule can also be applied to any traces where you want to minimize possible crosstalk/coupling.

An example is shown below where my RF trace was 0.313mm to produce a 50 Ohm impedance for a standard microstrip over ground plane (ie: type = single). Therefore, the RF trace to ground polygon pour clearance should be at least 0.939mm, which I have rounded up to 1mm.



NOTE: A keen observer may notice a clearance rule called Stitching GND in the example image above. Ignore this for now. This is autogenerated when GND via's are added (or stitched) all across your board, a procedure done later.

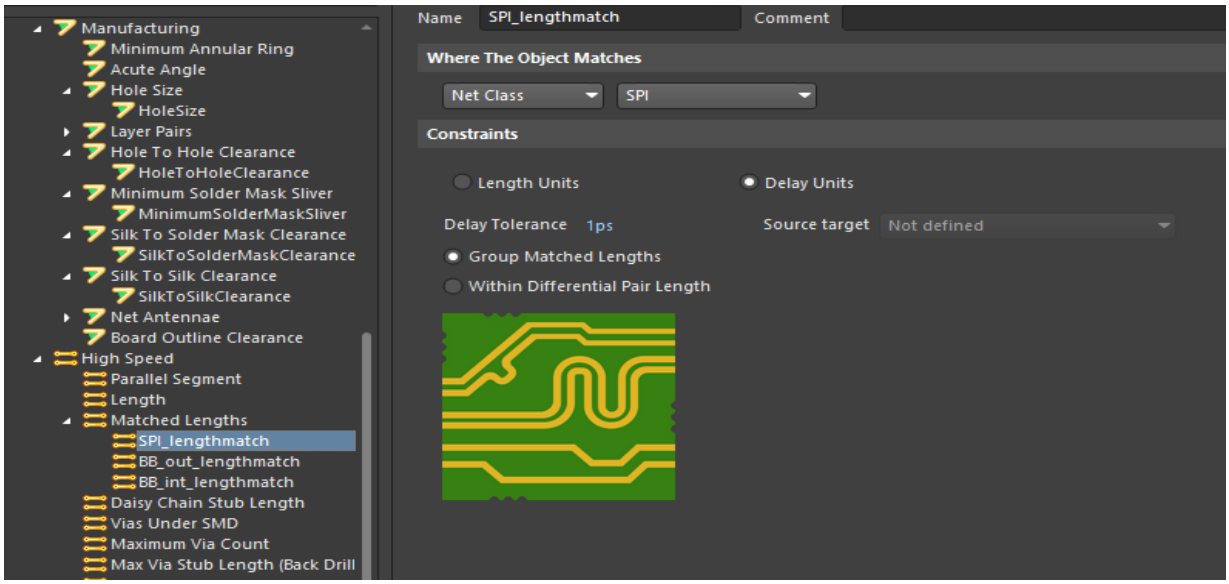
Similar procedure can be done for length matching DRC. In this case, I have not defined any nets as differential pair's at the schematic level, which may potentially eliminate the need to do this entirely (or not - worth an exploration!). Here, the goal is to make differential traces be approx. the same lengths to make sure the signals have no delay mismatch.

Go to DESIGN → RULES → HIGH SPEED → MATCHED LENGTHS

Then right click the "matched length" section and create new rule
-name the rule
-click into the new rule
-Under WHERE THE OBJECT MATCHES section select the left pulldown as "Net Class" and in the right pulldown select your Net Class of interest (ie: SPI)
-Under the CONSTRAINTS section, enter the tolerance (can either be a length tolerance or a delay tolerance).

I think in terms of time delay, and so I consider a good tolerance to be smaller than the signals approximate risetime (so for our signals on the order of single digit psec would be good) - once again likely overkill. This tolerance should be a function of how much clock skew/phase mismatch you are willing to handle and so putting it at the order of risetime in most cases should comfortably meet any clock skew / phase mismatch requirements.

An example is shown below:



In the layout tool, an interactive trace tuner is available. Additionally, the tool will indicate live once the trace has been tuned to within the custom design rule set.

To do so select the pointed to icon on the layout floating ribbon:

This is a pulldown menu from which you should select 'interactive length tuning'. If you are trying to tune a schematic defined differential pair, choose the second option in the pulldown (and the process is likely simpler).

Let's continue the discussion for the non-schematic defined differential pair trace that is to be tuned. **Once the interactive length tuning option is selected, click on the trace that is to be tuned (in this case choose the trace that is the shorter of the two differential nets, since the tuning will add length).**

A white box should appear that can be dragged. This will be the range in which the tuning can be done. If widened enough a mitred/square hump may appear which is the length tuning in action.

Left click to end the tuning. Go to the properties section with the white tuning box selected and you can change the tuning pattern style from Mitered Lines to Mitered Arc or rounded. I prefer rounded.

Note, the white tuning box can be adjusted both lengthwise and heightwise. This can be used to tune the trace with customizable "wiggling amplitudes" and different numbers of "wiggle cycles".

Recognize as you drag change the size of the white box and tuning is being done an indicator tells you if you are within the tuning tolerance set by DRC and also what the delay is (uses color coded indication to display if within DRC spec or not - green vs red).

7. Co-planar polygon pours (with now defined clearance rules, etc.)

Now that all routing and layout is complete, it is good to apply a polygon pour on the empty regions of the PCB for the routing layers. This will help with reducing EMI from affecting your signals and paths. It will also enhance your ground plane in various ways like lowering its resistance. It will also allow simple and automatic connections to be made for the pads that are to be connected to ground but have not yet actually been done so!

-To apply a polygon pour, make sure you are on the layer of interest (ie: top layer).
-Go to PLACE → POLYGON POUR
-Left click at the corners of the board to make the white outline cover the whole board
-Right click when complete
-click esc to apply pour to region
-double click on the pour and check its properties (make sure the net is GND) - if not define it as such and repour
-To repour, go to TOOLS → REPOUR → REPOUR ALL (or could do REPOUR SELECTED - and have selected the pour of interest). This should make the pour now be the GND net.
-Do the same thing for any other routing layers
***make sure that the 3*W rule is noticeable around RF traces to verify custom DRC is being followed**

IMPORTANT: Usually the polygon pour should autoconnect to any pads that are supposed to connect to the ground net. Be careful around RF paths where the clearance between ground plane and traces is large. If for instance you want a capacitor in your matching network to be in shunt (and thus have one pad connect to ground) the polygon pour may not autoconnect the pad to ground due to our custom design rule. Therefore, these may have to be manually inspected and manually wired from the pad to the pour.

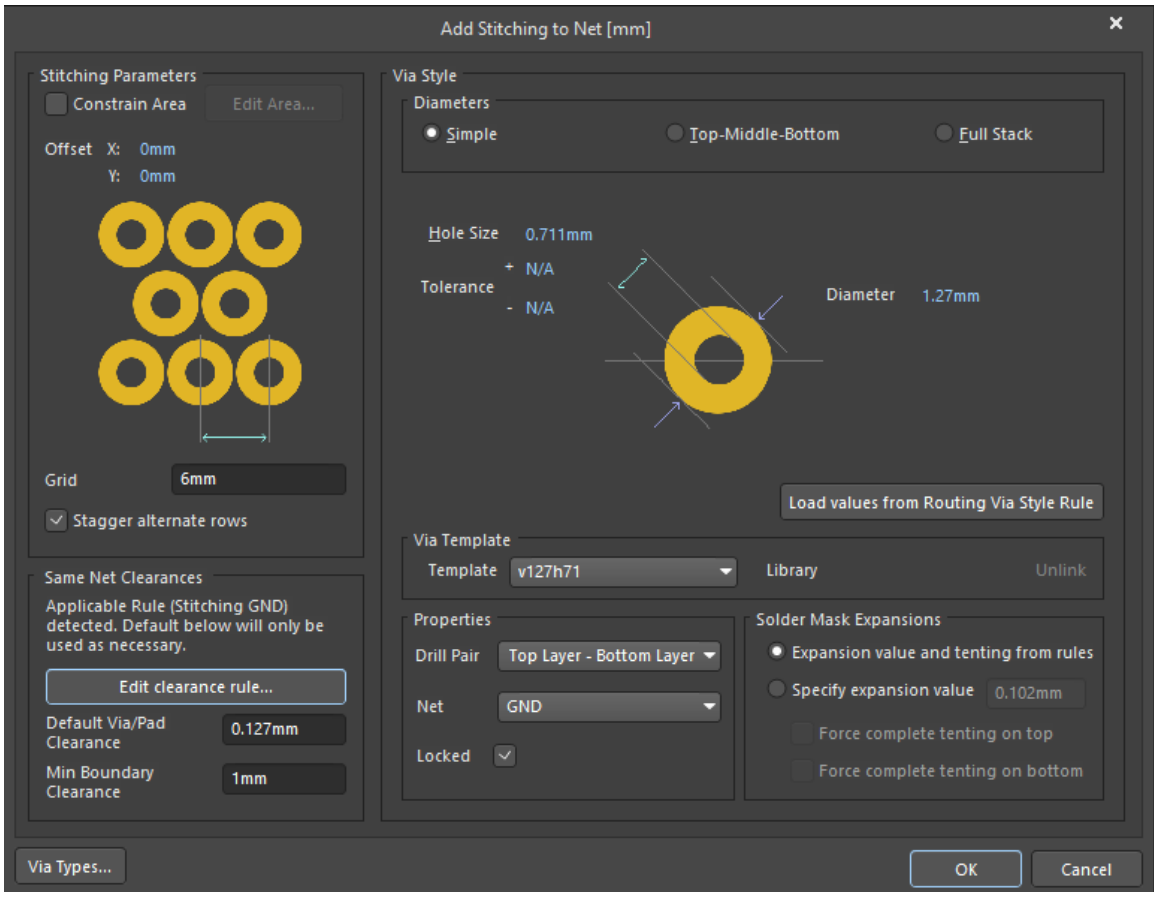
8. Apply gnd via stitching with spacing that is small enough to avoid RF resonances

Once ground polygon pours are completed we can perform via stitching. **I do my via stitching after the ground pour.** If you do it before and have a ground plane, the via's might get undesirable close to component pads, which I am sure there is a workaround for. Performing the via stitching after the polygon pour ensures that the via's will not get undesirably close to pads since the polygon pour sets a tighter constraint on where the via's are to be located.

To perform via stitching:
Go to TOOLS → VIA STITCHING/SHIELDING → ADD STITCHING TO NET…

Under stitch parameters define the Grid value. This is the center to center separation the stitching will try to be. This value can be selected by considering your highest RF frequency. Possible resonances in the board can occur, and **so a rule of thumb is to space your stitched via's no wider than one-tenth of a wavelength**. One-twentieth of a wavelength is optimal. This rule is more for RF shielding but seems to work well in general.

For example, I am operating at a 2.4GHz frequency with a relative dielectric of 4.2. Therefore, my guided wavelength is 60 mm. Thus, one tenth of that is 6mm, which is what is used as my grid space.



Also, beyond grid spacing, define the Net as GND to make sure the via is used for the ground net.

Click OK and the via's should be placed (might load for a bit).

Now the via's are placed, you will likely want to have thermal reliefs.

In order to apply such thermal reliefs, perform a "repour all". This can be done by going to TOOLS → POLYGON POURS → REPOUR ALL.

Now you will see some clearances of the polygon pour from the via's.

Extraction and Submission Files for PCBMinions

To extract the gerber file:

Files → Fabrication Output → Gerber Files

Click **OK** on popup box

Can ignore CAMtastic View (which simply shows the file that was extracted)

PCBMinions also requests a Drill Hole file which is extracted as shown below:

make sure to click back to the Layout .PCBDOC file

Files → Fabrication Output → NC Drill Files

Click **OK**

Note: you do not need to save the CAMtastic views as they are just viewing the extracted files. All the extracted files are autogenerated and placed in an OUTPUT file in the project that is named after the project name.

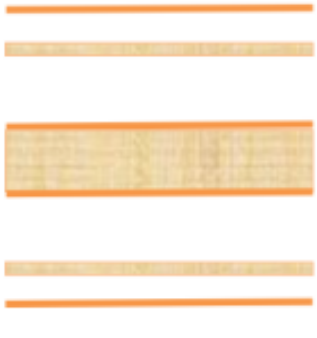
Zip the entire output file and upload it to fabricators website.

Appendix: PCBMinion Layer Stackup's (as of Aug 4, 2022)

PCB DESCRIPTION:4 LAYER PCB 1.6mm±0.1mm 1oz

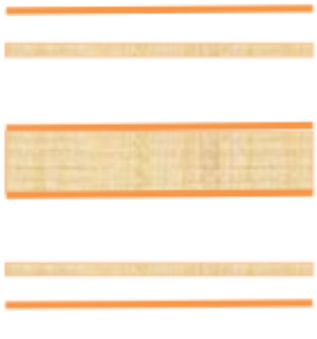
Copper	1	35 um	
Dielectric	1-2	0.175 mm (e.g. 1x Prepreg 7628 AT05 47% Resin) TG130 dielectric constant 4.2	
Copper	2	35 um	
Dielectric	2-3	1.13 mm (6x 7628M 43% Resin) TG150	dielectric constant 4.2
Copper	3	35 um	
Dielectric	3-4	0.175 mm (e.g. 1x Prepreg 7628 AT05 47% Resin) TG130 dielectric constant 4.2	
Copper	4	35 um	

PCB DESCRIPTION:4 LAYER PCB 1.2mm±0.1mm 1oz



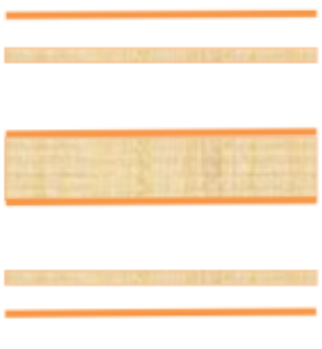
Copper	1	35 um	
Dielectric	1-2	0.175 mm (e.g. 1x Prepreg 7628 AT05 47% Resin) TG130 dielectric constant 4.2	
Copper	2	35 um	
Dielectric	2-3	0.73 mm (6x 7628M 43% Resin) TG150	dielectric constant 4.2
Copper	3	35 um	
Dielectric	3-4	0.175 mm (e.g. 1x Prepreg 7628 AT05 47% Resin) TG130 dielectric constant 4.2	
Copper	4	35 um	

PCB DESCRIPTION:4 LAYER PCB 1.0mm±0.1mm 1oz



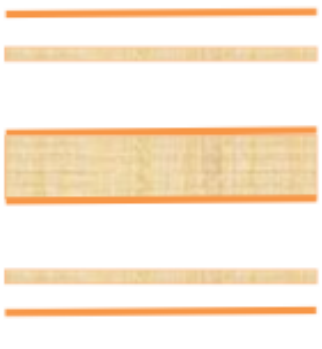
Copper	1	35 um	
Dielectric	1-2	0.175 mm (e.g. 1x Prepreg 7628 AT05 47% Resin) TG130 dielectric constant 4.2	
Copper	2	35 um	
Dielectric	2-3	0.53 mm (6x 7628M 43% Resin) TG150	dielectric constant 4.2
Copper	3	35 um	
Dielectric	3-4	0.175 mm (e.g. 1x Prepreg 7628 AT05 47% Resin) TG130 dielectric constant 4.2	
Copper	4	35 um	

PCB DESCRIPTION:4 LAYER PCB 0.8mm±0.1mm 1oz



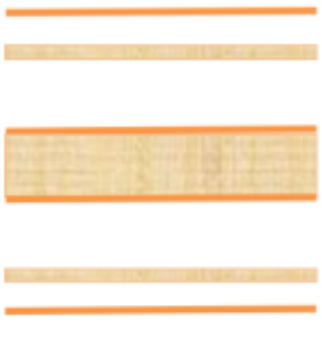
Copper	1	35 um	
Dielectric	1-2	0.175 mm (e.g. 1x Prepreg 7628 AT05 47% Resin) dielectric constant 4.2	TG130
Copper	2	35 um	
Dielectric	2-3	0.33 mm (6x 7628M 43% Resin) TG150 dielectric constant	4.2
Copper	3	35 um	
Dielectric	3-4	0.175 mm (e.g. 1x Prepreg 7628 AT05 47% Resin) dielectric constant 4.2	TG130
Copper	4	35 um	

PCB DESCRIPTION:4 LAYER PCB 0.6mm±0.1mm 1oz



Copper	1	35 um	
Dielectric	1-2	0.175 mm (e.g. 1x Prepreg 7628 AT05 47% Resin) dielectric constant 4.2	TG130
Copper	2	17 um	
Dielectric	2-3	0.17 mm (6x 7628M 43% Resin) TG150 dielectric constant	4.2
Copper	3	17 um	
Dielectric	3-4	0.175 mm (e.g. 1x Prepreg 7628 AT05 47% Resin) dielectric constant 4.2	TG130
Copper	4	35 um	

PCB DESCRIPTION:4 LAYER PCB 2.0mm±0.1mm 1oz



Copper	1	35 um	
Dielectric	1-2	0.175 mm (e.g. 1x Prepreg 7628 AT05 47% Resin) dielectric constant 4.2	TG130
Copper	2	35 um	
Dielectric	2-3	1.53 mm (6x 7628M 43% Resin) TG150 dielectric constant	4.2
Copper	3	35 um	
Dielectric	3-4	0.175 mm (e.g. 1x Prepreg 7628 AT05 47% Resin) dielectric constant 4.2	TG130
Copper	4	35 um	

Note:

Thin prepreg with thickness of 2.8-3.0mil is also available.

ADDITIONAL RESOURCE I FOUND THAT GOES OVER A BIT OF LAYER STACKUP AND IMPEDANCE PROFILER AND PROVIDES OTHER INFORMATION ON RF LAYOUT:

https://www.youtube.com/watch?v=8nSsCA_pB_c

-some things it covers:
***using Class to make sure RF widths are proper by referencing impedance profile (should autosize the net as well)**
***using coplanar routing to reduce trace width**
*** using vias and in RF paths (with properly autosized traces)**
+some other tricks!

General Altium Video Set:
https://www.youtube.com/c/AltiumAcademy

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Other things I could talk about:

-how to make the PCB board (reshape and define it) - also where the origin is
-silkscreen writing
-talk about adding drill holes at the PCB corners as a stand option for the PCB
-sma separation rule of thumb for ease of soldering (1 sma space away ~ 1cm)
-some schematic discussion (also how to make custom schematic component and footprints + libraries)
-talk about BOM and Manufacturing Part Search
-sma vs pin header debate